IN THE CLAIMS

1. A method for generating complex sinusoids of a desired frequency comprising the steps of:

multiplying a current phasor by a predetermined value (14) once every sampling interval to create a next phasor;

determining an error factor (26) for real and imaginary components of the next phasor; and

correcting the real and imaginary components by removing the error factor (28).

2. The method of claim 1 wherein the step of multiplying further comprises the step of:

identifying if a zero value condition exists (16) within either real or imaginary components of the next phasor and if the zero value condition exists not performing the steps of determining factor and correcting but instead performing a step substituting a complementary component of unity amplitude (18) to complex phasor components that exhibit the zero value condition.

3. The method of claim 2 wherein the step of multiplying further comprises the step of:

identifying if a condition of equality exits (20) between for real and imaginary components of the next phasor and if the conditions of equality exists not performing the steps of determining factor and correcting but instead performing a step of substituting an equal component (24) for both real and imaginary components of the next phasor.

4. The method of claim 3 wherein the step of identifying further comprises examining a plurality of highest order bits of the next phasor for the zero value condition or the condition of equality.

5. The method of claim 4 wherein the step of identifying further comprises examining the highest order bits of the next phasor to determine the zero value condition by determining if all the highest bits are either a logical 0 or a logical 1.

6 The method of claim 3 wherein the step of substituting further comprises substituting a components of a square-root of one-half unity amplitude for both real and imaginary components of the next phasor.

7. The method of claim 1 implemented within a systolic processor array.

8. The method of claim 1 implemented within a discrete logic device.

9. The method of claim 1 implemented as an algorithm running on a computer.

10. The method of claim 1 further comprising employing a sampling rate that is at least twice the desired frequency.

11. A method for generating complex sinusoids of a desired frequency comprising the steps of:

multiplying a current phasor by a predetermined value (14) once every sampling interval to create a next phasor;

identifying if the next phasor is integer multiple of 45 degrees (16, 20) and substituting at least one component (18, 24) within the next phasor if the next phasor is determined to be integer multiple of 45 degrees;.

determining an error factor (26) if the next phasor is not identified to be integer multiple of 45 degrees; and

correcting the real and imaginary components by removing the error factor (28).

12. The method of claim 12 wherein the step of identifying is performed by examining a plurality of highest order bits of the next phasor.

13. The method of claim 12 wherein the step of identifying further comprises identifying if a zero value condition exist (16) within either real or imaginary components of the next phasor and substituting a complementary component of unity amplitude to complex phasor components that exhibit the zero value condition.

14. The method of claim 12 wherein the step of identifying further comprises identifying if a condition of equality exits (20) between for real and imaginary components of the next phasor and if the conditions of equality exists substituting an equal component for both real and imaginary components of the next phasor.

15. The method of claim 14 wherein substituting further comprises substituting a square-root of one-half unity amplitude for both real and imaginary components of the next phasor.

16. A method for efficiently generating complex sinusoids of a desired frequency comprising the steps of:

implementing successive complex multiplications (14) upon a current phasor to create a plurality of next phasors; and

compensating for cumulative round-off errors (28) occurring within the next phasors.

17. The method of claim 16 wherein the step of compensating further comprises the step of examining a plurality of the most significant bit of the next phasors.

18. The method of claim 17 wherein the step of examining further comprises the steps of:

detecting a condition of zero value (16) within components of the next phasors; and

substituting a component of unity amplitude (18) to components of the next phasors for which the condition of zero value is detected.

19. The method of claim 16 wherein the step of examining further comprises the steps of:

detecting a condition of equal absolute-valued components (20) of the next phasors; and

substituting components of square-root one-half amplitude (24) to components of the next phasors that have been detected as having the condition of equal absolute-valued.

20. The method of claim 16 wherein the step of implementing further comprises employing a processor whose sampling rate that is at least twice the desired frequency.